# ADC-VX201
# User Manual

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# 1 About the Hardware

The ADC-VX201 is an Open VPX compliant and SOSA aligned XMC carrier designed to host Alpha Data FPGA mezzanine cards. The ADC-VX201 maps the hosted XMC to VITA 65 Slot Profile 14.6.11-0, supporting up to PCIe Gen5 (or equivalent) over the Data, Expansion, and Control Planes. Critically, the ADC-VX201 ensures that the mounted XMC is brought into alignment with the SOSA Technical Standard and hosts the required VITA 46.11 Tier 3 IPMC.

**VITA 65 Slot Profile**

- SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-0

**Supported Alpha Data XMCs**

- ADM-XRC-9Z1
- ADM-XRC-9R1
- ADM-XA210

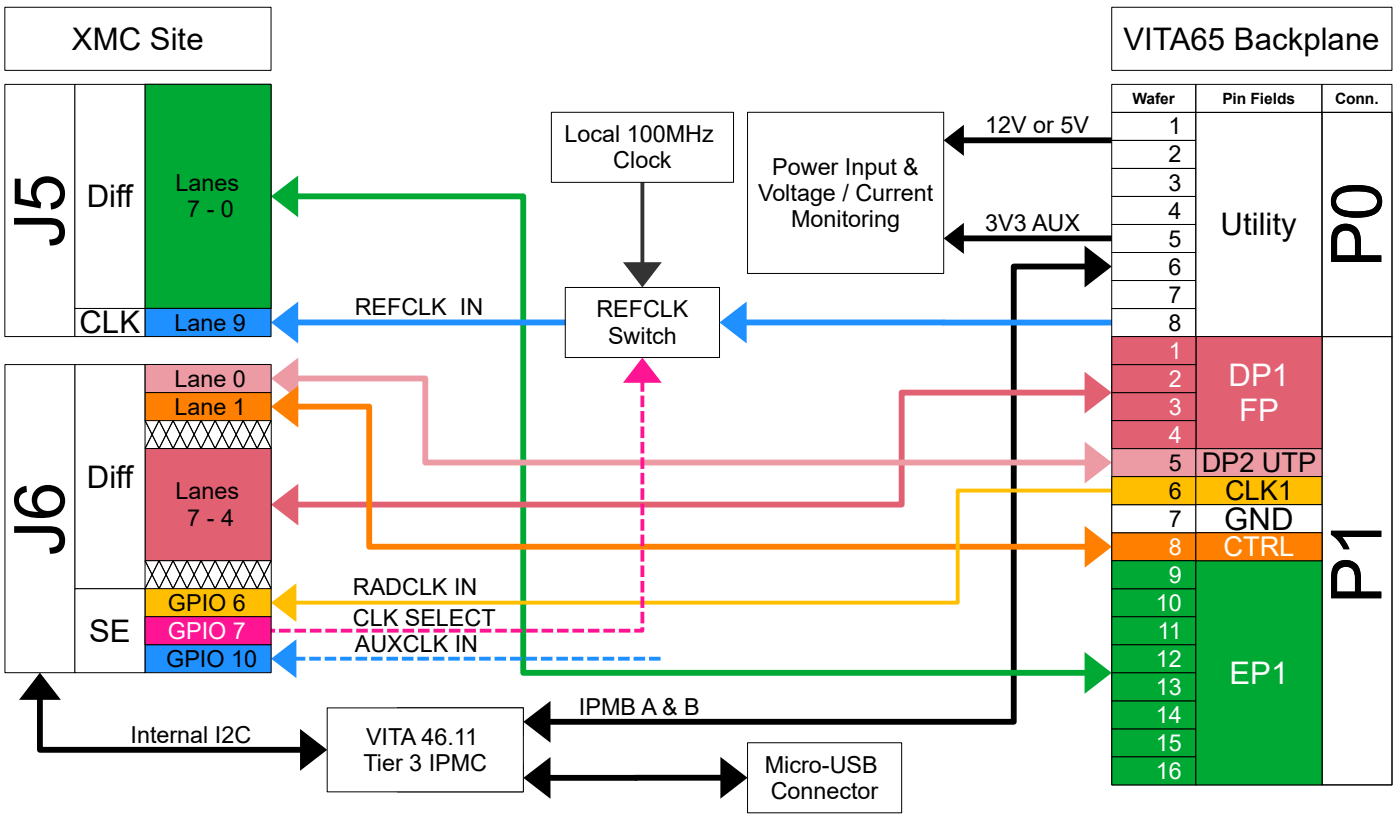


**Figure 1 : ADC-VX201 Block Diagram**

# 2 Board Features

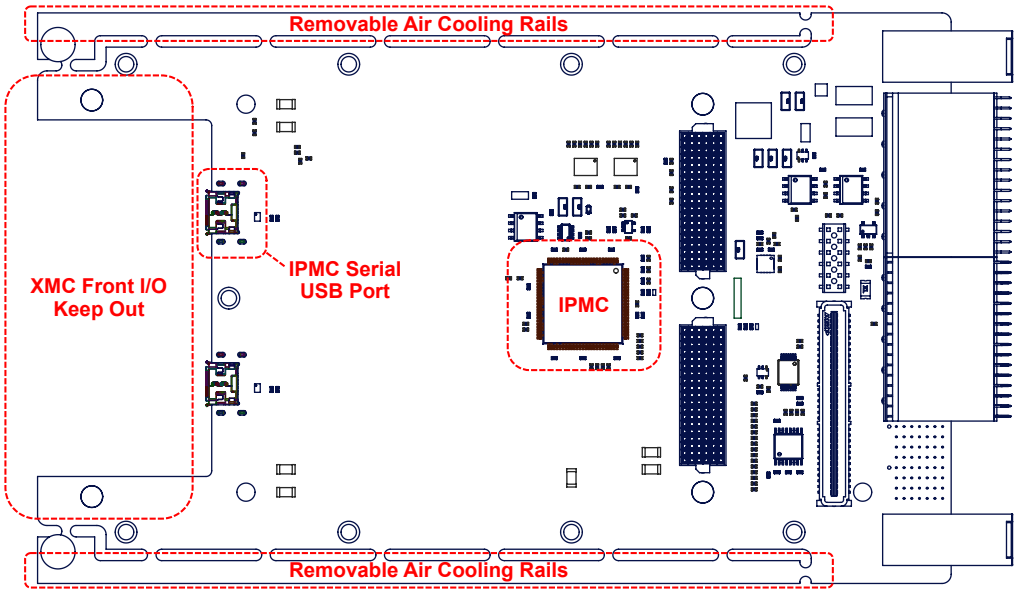


**Figure 2 : Top Side Features**

## 2.1 Power

The ADC-VX201 requires the 12V and 3V3_AUX supplies from the VPX backplane.

The 5V supply from the VPX backplane is disconnected by default but can be enabled via a build option. Please contact sales@alpha-data.com for details.

The ADC-VX201 generates the 3V3 supply for the XMC site using the primary power input from the VPX backplane.

The 3V3 supply can be used to provide 3V3_AUX via a build option. Please contact sales@alpha-data.com for details.

The ADC-VX201 monitors the current and voltage of the 12V, 3V3 and 3V3_AUX rails. The readings can be accessed via the IPMC or probed at the test points on the back of the board.

## 2.2 High-Speed Serial I/O

### 2.2.1 Data Planes

The ADC-VX201 provides two Data Planes. Data Plane 1 (DP1) consists of 1 Fat Pipe (FP) and Data Plane 2 (DP2) consists of 1 Ultra-Thin Pipe (UTP). DP1 is connected to lanes [7:4] of XMC J6, while DP2 is connected to lane 0 of XMC J6.

### 2.2.2 Expansion Plane

The ADC-VX201 provides one Expansion Plane. Expansion Plane 1 (EP1) a Double Fat Pipe (DFP) connected to lanes [7:0] of J5. EP1 can be repartitioned into 2 FP's in accordance with VITA 65.

### 2.2.3 Control Plane

The ADC-VX201 provides one Control Plane. Control Plane 1 (CP1) consists of 1 Ultra-Thin Pipe connected to lane 1 of XMC J6.

## 2.3 Clocking

### 2.3.1 REFCLK

The ADC-VX201 provides the bussed VPX REFCLK (Reference Clock) to the primary clock input (J5.A19 and J5.B19) of the XMC site.

An on-board 100MHz clock is also provided. The user can choose between the bussed REFCLK or the on-board solution by toggling GPIO7 (J6.C16) of the XMC site, or through enabling (switch ON) on-board switch SW1-1.

### 2.3.2 AUXCLK

The ADC-VX201 forwards the VPX AUXCLK (Auxillary Clock) to GPIO10 (J6.F15) of the XMC site.

### 2.3.3 RADCLK

The ADC-VX201 forwards the VPX RADCLK (Radial Clock) to GPIO6 (J6.F17) of the XMC site.

## 2.4 System Control Signals and Low Speed I/O

All system control signals are buffered on the ADC-VX201 and therefore require 3.3V_AUX to be present. The states of SYSCON, SYSRESET, NVMRO, and GDiscrete1 are monitored by the IPMC and can be read via the USB interface.

### 2.4.1 System Controller (SYSCON)

The ADC-VX201 supports the System Controller signal from the VPX backplane. The SYSCON signal from P1 is fed into XMC ROOT0 (J5.E19).

The SYSCON signal can also be asserted through software by toggling GPIO1 (J6.C19) of the XMC site.

### 2.4.2 System Reset (SYSRESET)

The ADC-VX201 supports the System Reset signal from the VPX backplane.

SYSRESET is mapped to the MRSTI pin (J5.F2) of the XMC site, and is input only.

### 2.4.3 Module Maskable Reset (MSKRST)

The MSKRST signal is connected to SYSRESET on the ADC-VX201, meaning it can be used as a secondary SYSRESET input. This signal is input only.

### 2.4.4 Non-Volatile Memory Read Only (NVMRO)

The NVMRO signal is mapped from the backplane to the MVMRO pin (J5.C16) of the XMC site. This signal is input only.

### 2.4.5 System Management Buses (SM[3:0])

The System Management Buses are used as the VITA 46.11 Intelligent Platform Management Buses (IPMB A & B). Both buses are buffered on-board and connect to the IPMC.

### 2.4.6 JTAG

The ADC-VX201 supports JTAG from the VPX backplane. The JTAG signals are passed to the XMC site.

### 2.4.7 Bussed GPIO (GDiscrete1)

The ADC-VX201 supports the optional GPIO GDiscrete1 from the VPX backplane. This signal is input only and is connected to GPIO 8 (J6.C18) of the XMC site.

# 2.5 Intelligent Platform Management Controller (IPMC)

The ADC-VX201 hosts an on-board microcontroller which acts as a VITA 46.11 Tier-3 IPMC. The microcontroller monitors the system health and manages the Intelligent Platform Management Buses (IPMB-A and IPMB-B).

There are two methods to interface with the microcontroller. Either through the micro-USB port at the front edge of the board, or through the IPMB.

The micro-USB is intended to be used with the Alpha Data utility AVR2UTIL which can be downloaded from https://alpha-data.com/resources/drivers-apis-and-software-utilities/. Once installed on a host PC, AVR2UTIL can be run with the following option to see the available commands:

```
avr2util -?
```

The other method to interface with the microcontroller is through the IPMB. Both IPMB-A and IPMB-B become immediately available upon power on, unless SW1-3 or S1-4 are switched on. For more information on the switches see Section 2.6.

## 2.5.1 Intelligent Platform Management Interface (IPMI)

The on-board IPMC communicates with the VPX system chassis manager via the IPMB. The supported IPMI commands are given in Table 1. Supported commands defined in VITA 46.11 are given in Table 2.

| Command Name | IPMI Specification Section | NetFn | CMD |
|---|---|---|---|
| Get Device ID | 1.5:17.1 | App (06h) | 01h |
| Cold Reset | 1.5:17.2 | App (06h) | 02h |
| Warm Reset | 1.5:17.3 | App (06h) | 03h |
| Get Self Test Results | 1.5:17.4 | App (06h) | 04h |
| "Broadcast" "Get Device ID" | 1.5:17.9 | App (06h) | 01h |
| **BMC Device and Messaging Commands** | | | |
| Set BMC Global Enables | 1.5:18.1 | App (06h) | 2Eh |
| Get BMC Global Enables | 1.5:18.2 | App (06h) | 2Fh |
| Send Message | 1.5:18.7 | App (06h) | 34h |
| Master Write/Read | 1.5:18.10 | App (06h) | 52h |
| **Event Commands** | | | |
| Set Event Receiver | 1.5:23.1 | S/E (04h) | 00h |
| Get Event Receiver | 1.5:23.2 | S/E (04h) | 01h |
| Platform Event (a.k.a “Event Message”) | 1.5:23.3 | S/E (04h) | 02h |
| **Sensor Device Commands** | | | |
| Get Device SDR Info | 1.5:29.2 | S/E (04h) | 20h |
| Get Device SDR | 1.5:29.3 | S/E (04h) | 21h |
| Reserve Device SDR Repository | 1.5:29.4 | S/E (04h) | 22h |
| Set Sensor Event Enable | 1.5:29.10 | S/E (04h) | 28h |

**Table 1 : Supported IPMI Commands (continued on next page)**

| Command Name | IPMI Specification Section | NetFn | CMD |
|---|---|---|---|
| Get Sensor Event Enable | 1.5:29.11 | S/E (04h) | 29h |
| Get Sensor Reading | 1.5:29.14 | S/E (04h) | 2Dh |
| **FRU Device Commands** | | | |
| Get FRU Inventory Area Info | 1.5:28.1 | Storage (0Ah) | 10h |
| Read FRU Data | 1.5:28.2 | Storage (0Ah) | 11h |
| Write FRU Data | 1.5:28.3 | Storage (0Ah) | 12h |
| **SEL Device Commands** | | | |
| Get SEL Info | 1.5:25.2 | Storage (0Ah) | 40h |
| Reserve SEL | 1.5:25.4 | Storage (0Ah) | 32h |
| Get SEL Entry | 1.5:25.5 | Storage (0Ah) | 43h |
| Clear SEL | 1.5:25.9 | Storage (0Ah) | 47h |
| Get SEL Time | 1.5:25.10 | Storage (0Ah) | 48h |
| Set SEL Time | 1.5:25.11 | Storage (0Ah) | 49h |

**Table 1 : Supported IPMI Commands**

All VITA 46.11 defined commands use NetFn equal to "Group Extension" (2Ch / 2Dh) and Group ID equal to the VITA-reserved Group ID of 03h.

| Command Name | VITA 46.11 Section | NetFn | CMD |
|---|---|---|---|
| Get VSO Capabilities | 10.1.3.1 | Group Extension (2Ch) | 00h |
| FRU Control | 10.1.3.6 | Group Extension (2Ch) | 04h |
| Set IPMB State | 10.1.3.7 | Group Extension (2Ch) | 09h |
| Set FRU State Policy Bits | 10.1.3.9 | Group Extension (2Ch) | 0Ah |
| Get FRU State Policy Bits | 10.1.3.8 | Group Extension (2Ch) | 0Bh |
| Set FRU Activation | 10.1.3.8 | Group Extension (2Ch) | 0Ch |
| Get Device Locator Record ID | 10.1.3.8 | Group Extension (2Ch) | 0Dh |
| FRU Control Capabilities | 10.1.3.18 | Group Extension (2Ch) | 1Eh |
| Get FRU Address Info | 10.1.3.3 | Group Extension (2Ch) | 40h |
| Get Mandatory Sensor Numbers | 10.1.3.25 | Group Extension (2Ch) | 44h |
| Get FRU Hash | 10.1.3.31 | Group Extension (2Ch) | 45h |
| Get Payload Mode Capabilities | 10.1.3.32 | Group Extension (2Ch) | 46h |
| Set Payload Mode | 10.1.3.33 | Group Extension (2Ch) | 47h |

**Table 2 : Supported VITA 46.11 Defined Commands**

## 2.6 Switch Definitions

There are 4 switches on the underside of the board at Switch SW1. The location is shown in Figure 3 The purpose of each switch is defined in Table 3.

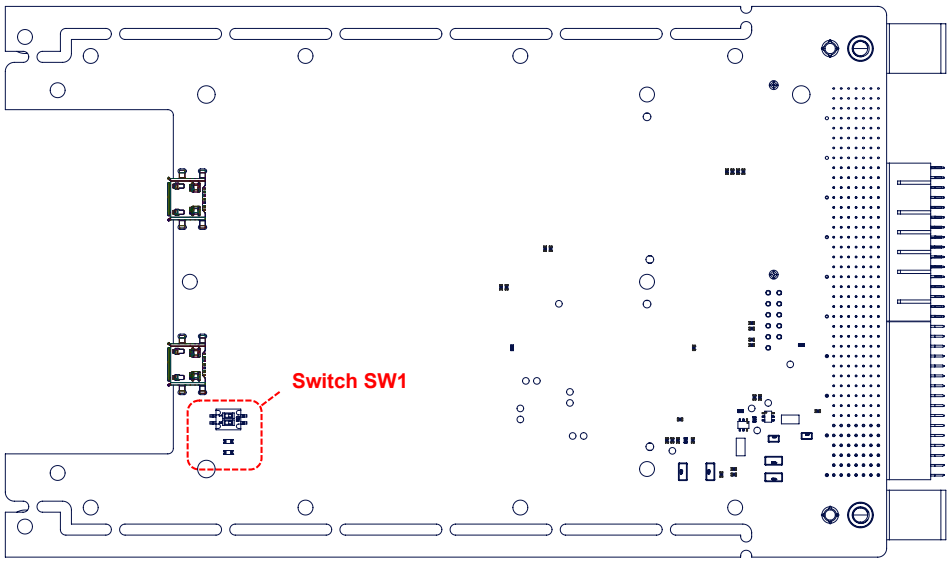


**Figure 3 : SW1 Switch Location**

| Switch Ref. | Silkscreen | Function | ON State | Off State |
|---|---|---|---|---|
| SW1-1 | SW1A-CLK_SEL | REFCLK Select | VPX bussed clock | Local clock |
| SW1-2 | SW1B-FW_UPDT | Reserved for Alpha Data internal use | | |
| SW1-3 | SW1C-IPMB0_EN | IPMB-A Disable | IPMB-A disabled | IPMB-A enabled |
| SW1-4 | SW1C-IPMB1_EN | IPMB-B Disable | IPMB-B disabled | IPMB-B enabled |

**Table 3 : SW1 Switch Definitions**

## 2.7 VPX Mechanical Keying

The ADC-VX201 is delivered with the VPX guides unkeyed. For custom keying options please contact sales@alpha-data.com.

# 3 Supported XMC Modules

The ADC-VX201 supports the following Alpha Data XMC modules -

- ADM-XRC-9Z1 - Zynq Ultrascale+ MPSoC
- ADM-XRC-9R1 - Zynq Ultrascale+ RFSoC
- ADM-XA210 - Versal AI Core and Versal Prime

The mapping of these XMCs onto the VPX backplane is best described in the VPX notation as defined in Section 2.2. The mapping of each XMC into the Data, Expansion, and Control Planes is defined in Table 4.

| XMC | Dataplane 1 | Dataplane 2 | Expansion Plane | Control Plane |
|---|---|---|---|---|
| ADM-XRC-9Z1 | MGT229 [3:0] | MGT228 [0] | MGT227 & [3:0] MGT226 [3:0] | MGT228 [1] |
| ADM-XRC-9R1 | MGT128 [3:0] | MGT129 [3] | MGT505 [3:0] | MGT129 [2] |
| ADM-XA210 | GTY204 [3:0] | GTY203 [0] | GTY103 [3:0] & GTY104 [3:0] | GTY203 [1] |

**Table 4 : XMC GT Mapping**

# 4 Cooling Option

The ADC-VX201 is designed to fully accommodate both air cooled and conduction cooled chassis both with and without front IO.

## 4.1 Air Cooled

Two removable tabs along the sides of board allow for easy insertion into standard air cooled chassis. Due to extremely low power consumption this carrier does not require a heatsink in the air cooled configuration.

The removable tabs can be replaced by metal tabs if a customer requires a board that can be both air cooled and conduction cooled during its lifetime.

## 4.2 Conduction Cooled

A Vita 48.2 compliant conduction cooled frame will ship with the board for conduction cooled applications.

Custom conduction cooling assemblies can be designed to optimize heat transfer from critical components to the side rails as needed. Please contact sales@alpha-data.com for details.

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# Appendix A: Carrier Connector Pin Assignments

| Wafer | Row G | Row F | Row E | Row D | Row C | Row B | Row A |
|---|---|---|---|---|---|---|---|
| 1 | 12V0 | 12V0 | 12V0 | - | - | - | - |
| 2 | 12V0 | 12V0 | 12V0 | - | - | - | - |
| 3 | 5V0* | 5V0* | 5V0* | - | 5V0* | 5V0* | 5V0* |
| 4 | IPMB_SCL_B | IPMB_SDA_B | GND | - | GND | SYSRESET | NVMRO |
| 5 | GAP | GA4 | GND | 3V3_AUX | GND | IPMB_SCL_A | IPMB_SDA_A |
| 6 | GA3 | GA2 | GND | - | GND | GA1 | GA0 |
| 7 | JTAG_TCK | GND | JTAG_TDO | JTAG_TDI | GND | JTAG_TMS | - |
| 8 | GND | REFCLK_N | REFCLK_P | GND | AUXCLK_N | AUXCLK_P | GND |

**Table 5 : P0 Pin Assignments**

* Requires build option.

| Wafer | Row G | Row F | Row E | Row D | Row C | Row B | Row A |
|---|---|---|---|---|---|---|---|
| 1 | GDISC1 | GND | J6_TX4_N | J6_TX4_P | GND | J6_RX4_N | J6_RX4_P |
| 2 | GND | J6_TX5_N | J6_TX5_P | GND | J6_RX5_N | J6_RX5_P | GND |
| 3 | - | GND | J6_TX6_N | J6_TX6_P | GND | J6_RX6_N | J6_RX6_P |
| 4 | GND | J6_TX7_N | J6_TX7_P | GND | J6_RX7_N | J6_RX7_P | GND |
| 5 | SYSCON | GND | J6_TX0_N | J6_TX0_P | GND | J6_RX0_N | J6_RX0_P |
| 6 | GND | RADCLK_N | RADCLK_P | GND | MP01-TD | MP01-RD | GND |
| 7 | GND | GND | GND | GND | GND | GND | GND |
| 8 | GND | J6_TX1_N | J6_TX1_P | GND | J6_RX1_N | J6_RX1_P | GND |
| 1 | MP02-TD | GND | PCIE_TX0_N | PCIE_TX0_P | GND | PCIE_RX0_N | PCIE_RX0_P |
| 2 | GND | PCIE_TX1_N | PCIE_TX1_P | GND | PCIE_RX1_N | PCIE_RX1_P | GND |
| 3 | MP02-RD | GND | PCIE_TX2_N | PCIE_TX2_P | GND | PCIE_RX2_N | PCIE_RX2_P |
| 4 | GND | PCIE_TX3_N | PCIE_TX3_P | GND | PCIE_RX3_N | PCIE_RX3_P | GND |
| 5 | - | GND | PCIE_TX4_N | PCIE_TX4_P | GND | PCIE_RX4_N | PCIE_RX4_P |
| 6 | GND | PCIE_TX5_N | PCIE_TX5_P | GND | PCIE_RX5_N | PCIE_RX5_P | GND |
| 7 | MSKRST | GND | PCIE_TX6_N | PCIE_TX6_P | GND | PCIE_RX6_N | PCIE_RX6_P |
| 8 | GND | PCIE_TX7_N | PCIE_TX7_P | GND | PCIE_RX7_N | PCIE_RX7_P | GND |

**Table 6 : P1 Pin Assignments**

# Revision History

| Date | Revision | Changed By | Nature of Change |
|---|---|---|---|
| 07 Apr 2025 | 0.1 | J. Wood | Preliminary |

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